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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,277	07/08/2003	Thomas R. Bednar	BUR920020092US1	1276
30449	7590	03/11/2005	EXAMINER	
SCHMEISER, OLSEN + WATTS 3 LEAR JET LANE SUITE 201 LATHAM, NY 12110			TAT, BINH C	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/604,277	BEDNAR ET AL	
<b>Examiner</b>	<b>Art Unit</b>	2825	
Binh C. Tat			

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 17 December 2004.  
2a) This action is FINAL.                            2b) This action is non-final.  
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 21-40 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) Claim(s) \_\_\_\_\_ is/are allowed.  
6) Claim(s) 21-40 is/are rejected.  
7) Claim(s) \_\_\_\_\_ is/are objected to.  
8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
10) The drawing(s) filed on 08 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) Notice of References Cited (PTO-892)  
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) Notice of Informal Patent Application (PTO-152)  
6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

This is a response to the response filed on 12/21/04. The applicant argument regarding Buffet et al are not persuasive; therefore, all the rejections based on Buffet et al are retained and repeated for the following reasons.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Buffet et al. (U.S Patent 6631502).
3. As to claims 21, and 31, Buffet et al. disclose an electrical structure comprising: a parent terrain denoted as V0 (see fig 2 element 120 col 5 lines 35-41); and N voltage islands denoted as V1, Mz, . . . , Vx nested within said parent terrain, N at least 2 (see fig 2 element 110 col 5 lines 42-45), voltage island Vz nested within a voltage island Vz-1 for Z=1, 2,..., N. 22 (see fig 2 element 105 col 5 lines 45-56).
4. As to claims 22, and 32, Buffet et al. disclose wherein each voltage island of the N voltage island includes one or more voltage power supplies selected from the group consisting of an internal voltage island VDDI power supply, an externally supplied state saving VDDSS

power supply, an externally supplied VDDN power supply, and combinations thereof (see fig 1 fig 2 col5 lines 11-30).

5. As to claims 23, and 33, Buffet et al. disclose wherein said one or more power supplies of voltage island  $V_x$  for  $X_r - z_l$ ,  $2, \dots, N$  are each independently coupled to one of (a) said one or more power supplies of voltage island  $V_y$  for  $Y=1, 2, \dots, N$ ,  $X$  not equal to  $Y$ , (b) a VDDO power supply of said parent terrain or (c) one or more external to said parent terrain power supplies (see fig 1 fig 2 and fig 3 col5 lines 11-30 and line 57 to col 6 lines 8).

6. As to claims 24, and 34, Buffet et al. disclose wherein each voltage island of the  $N$  voltage islands includes (a) an externally supplied VDDN power supply and a voltage shifting means, or (b) said externally supplied VDDN power supply and a fencing means or (c) said externally supplied VDDN power supply, said voltage shifting means and said fencing means (see fig 2-4 and fig 9a-9b col 5 lines 11 to col 6 lines 60 and col 8 lines 30 lines 30 to col 9 lines 42).

7. As to claims 25, and 35, Buffet et al. disclose wherein said fencing means comprises logic latches (see fig 2-4 and fig 9a-9b col 5 lines 11 to col 6 lines 60 and col 8 lines 30 lines 30 to col 9 lines 42 and background).

8. As to claims 26, and 36, Buffet et al. disclose wherein each voltage island of the  $N$  voltage islands further includes one or more substructures selected from the group consisting of (a) an internal voltage island VDDI power distribution network, (b) state saving means, (c) one or more switching elements coupled between said externally supplied VDDN power supply and said internal voltage island VDDI power distribution network, and (d) one or more voltage

buffering circuit (see fig 2-4 and fig 9a-9b col 5 lines 11 to col 6 lines 60 and col 8 lines 30 lines 30 to col 9 lines 42).

9. As to claims 27, and 37, Buffet et al. disclose wherein said one or more switching elements is selected from the group consisting of hard connections, voltage regulators headers and footers (see fig 2-4 and fig 9a-9b col 5 lines 11 to col 6 lines 60 and col 8 lines 30 lines 30 to col 9 lines 42 and background).

10. As to claims 28, and 38, Buffet et al. disclose wherein said state saving means includes at least one state saving latch (see fig 2-4 and fig 9a-9b col 5 lines 11 to col 6 lines 60 and col 8 lines 30 lines 30 to col 9 lines 42 and background)

11. As to claims 29, and 39, Buffet et al. disclose wherein one or more voltage islands of the N voltage islands further includes a power management state machine coupled to an internal voltage island VDDI power supply distribution network, said power management state machine of voltage island Vx for X=1, 2, . . . , N located in (a) voltage island Vv for Y=1, 2, . . . , N, Y less than X, or (b) in said parent terrain (see fig 1 fig 2 and fig 3 col5 lines 11-30 and line 57 to col 6 lines 8.

12. As to claims 30, and 40, Buffet et al. disclose wherein said parent terrain is an integrated circuit chip or a voltage island within said integrated circuit chip (see fig 2 element 120 col 5 lines 35-41).

***Response to Amendment and Arguments***

Applicant's arguments filed December 17<sup>th</sup>, 2004 have been fully considered but they are not persuasive.

Applicant contends that Buffet et al do not describe "a parent terrain denoted as V0; and N voltage islands denoted as V1, Mz, . . . , Vx nested within said parent terrain, N at least 2, voltage island Vz nested within a voltage island Vz-1 for Z=1, 2,..., N. 22" probes as claimed. In response to Applicant's argument that Buffet et al do not describe "a parent terrain denoted as V0; and N voltage islands denoted as V1, Mz, . . . , Vx nested within said parent terrain, N at least 2, voltage island Vz nested within a voltage island Vz-1 for Z=1, 2,..., N. 22" probes as claimed, Examiner respectfully disagrees. Applicant is directed to a parent terrain denoted as V0 (see fig 2 element 120 col 5 lines 35-41); and N voltage islands denoted as V1, Mz, . . . , Vx nested within said parent terrain, N at least 2 (see fig 2 element 110 col 5 lines 42-45), voltage island Vz nested within a voltage island Vz-1 for Z=1, 2,..., N. 22 (see fig 2 element 105 col 5 lines 45-56). For this reason, examiner holds the rejection proper.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

1. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BINH TAT  
Art Unit 2825  
March 5, 2005



VUTHE SIEK  
PRIMARY EXAMINER